Notice of Allowability	Application No.	Applicant(s)	
	10/738,405	YAUNG ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 30 Mar 2006 (Cert. of Mailing date: 28 Mar 2006).*.

2. ☒ The allowed claim(s) is/are *1-12,14-17 and 22-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *See Continuation Sheet*.

John B. Vigushin
Primary Examiner
Art Unit: 2841

Continuation of Attachment(s) 9. Other: A copy of UK Patent Application GB 2123621 A.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed March 30, 2006 (Certificate of Mailing date: March 28, 2006). The Examiner acknowledges the amendments to Claims 1 and 9, and the cancellation of Claims 13 and 18-21. Accordingly, Claims 1-12, 14-17 and 22-25 remain pending in the instant amended Application.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In the transcription of the subject matter from now-cancelled Claim 13 incorporated into base Claim 1 by amendment, the Examiner has noted a typographical error which the Examiner has corrected by Examiner's Amendment. Accordingly, the application has been amended as follows:

In Claim 1, line 11: "for" has been changed to --by--.

[*Examiner's Note*: By this amendment to Claim 1, lines 10-12 of the claim now read as "wherein the circuit board is connected to another circuit board ~~for~~ by a first half part..."].

Allowable Subject Matter

3. Claims 1-12, 14-17 and 22-25 have been allowed.

4. The following is an examiner's statement of reasons for allowance:

As to Claims 1-12, patentability resides in **the combination of** *a first half part of the male interlocking element of the circuit board connector inserted into the female interlocking element of the circuit board* **and** *a second half part of the male interlocking element of the circuit board connector inserted into a female interlocking element of the another circuit board*, in further combination with the other limitations of base Claim 1.

As to Claims 14-17, patentability resides in **the combination of** *at least one male interlocking element connected to the body, a first half part of the male interlocking element capable of being inserted into the first female interlocking element* **and** *a second half part of the male interlocking element capable of being inserted into the second female interlocking element*, in further combination with the other limitations of base Claim 14.

As to Claims 22-24, patentability resides in **the combination of** *male interlocking means connected to the body means, a first half part of the male interlocking means capable of being inserted into the first female interlocking means* **and** *a second half part of the male interlocking means capable of being inserted into the second female interlocking means*, in further combination with the other limitations of base Claim 22.

As to Claim 25, patentability resides in **the combination of** *inserting a first half part of the male interlocking element into the first female interlocking element* **and**

inserting a second half part of the male interlocking element into the second female interlocking element, in further combination with the other limitations of the claim.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Allowed Claims 1-12, 14-17 and 22-25 will be renumbered as Claims 1-20, respectively, for publication in the issued patent.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Clark (GB 2123621 A) discloses a connector 1 with bolts 3 and nuts 7 that engage recesses 17, 18, 20 of circuit board 19, the bolts 3 and nuts 7 establishing either of an electrical or a mechanical connection between board 19 on one side and another board 19 on the other side of connector 1 (Figs. 1-7). There is no interlocking relationship between bolt 3 and a recess 17, 18 , 20; the locking action between any two boards 19 being performed by nuts 7, and not requiring any supplemental interlocking features between the connector 1 and boards 19. Further disclosed is an alignment projection 22 that is integrally molded into the body of connector 1, such that half of projection 22 is inserted in recess 23 of board 19 (shown in Fig. 7) and the other half is inserted in recess 23 of another board 19 on the other side of connector 1, in order that

the boards 19 are properly positioned for electrical connection on each side. So alignment projection 22 functions as a connection key to ensure proper alignment and electrical connection of the two boards 19 (p.3, col.1: 12-30). Note that Clark merely teaches that the projection 22 "is arranged to extend into" the recess (channel) 23 (p.3, col.1: 12-16) and does not teach or fairly suggest that there is an interference fit or any other kind of concomitant structural interlocking occurring between the projection 22 and recess 23 during positioning of boards 19 onto connector 1 (p.3, col.1: 16-22), wherein projection 22 would function as some kind of "male" interlock element and recess 23 as a "female" interlock element as part of the alignment function; neither does Clark suggest a necessity of such an interlock structure nor motivate a benefit of a such a structure between alignment elements 22 and 23, since the locking function between two boards 19 interconnected by connector 1 is structurally effected by the nuts 7 and furthermore, Clark teaches that only one such projection 22 is required (Fig. 7) between any two boards 19 in order to perform the keying and alignment functions (p.3, col.1: 22-30). Thus, there is no evidence or sufficient motivation in Clark for considering connector projection 22 to be a "male" element and board recess 23 to be a "female" element in an interlocking relationship for structural securement or for keying purposes.

b) Pearson et al. (US 6,801,436 B2) discloses an extension strip 60 for facilitating the mounting of overhanging components 15 onto one end of circuit board 50, the extension strip 60 having male interlocking elements (or "keys") 62 that are inserted into female interlocking elements (or "keyholes") 52, on the edge of circuit 50 whence the components 15 overhang, for establishing a secure mechanical connection between

strip 60 and board 50 during the component mounting process (Figs. 2 and 3; col.3: 51-58; col.4: 3-7 and 24-34).

c) Mori et al. (US 5,834,843) discloses, in Fig. 5A, a "dumbbell" shaped connector functioning, apparently, as a male interlocking element 35 comprising two half parts, wherein two semiconductor chips 32 (not circuit boards; col.4: 24-40) respectively have female interlocking elements (recessed terminals 33a) into which each respective half part of the male interconnecting element 35 is inserted to electrically and mechanically interconnect the adjacent chips 32 (col.5: 38-51; an interlocking structure is not explicitly taught but may be inferred from col.5: 47-51). The embodiment of Fig. 9B discloses that a supplemental chip may also be surface-mounted onto chip 32 in order to add functionality, such as extra memory capacity, to chip 32, and the resultant chip-on-chip structure mounted onto a motherboard 38 (as in Fig. 9B; col.7: 39-44) or another motherboard 38 (as in Figs. 7A,B; col.6: 44-61) in order to complete the package. Mori et al. most certainly does not teach or fairly suggest that the motherboards 38, upon which chips 32 are mounted, can be so interconnected with other circuit boards or motherboards, electrically and/or mechanically, by such unitary and singly applied "dumbbell" shaped connectors 35, and also does not teach or fairly suggest that the chips 32, themselves, may be modified to be circuit board structures so interconnected with other circuit boards, electrically and/or mechanically, by such unitary and singly applied "dumbbell" shaped connectors 35 for at least the reason that, were the chips 32 to be modified to be circuit boards instead, then the above-mentioned embodiment of an interconnected set of chip-on-chip structures, as contemplated by

Mori et al., would be eliminated, resulting in the loss of the functional enhancement they provide, e.g., extra memory capacity, to the semiconductor devices 32 so coupled, as contemplated by Mori et al.

d) Chia et al. (US 6,512,293 B1) discloses, in Figs. 1 and 2, interlocking semiconductor BGA packages (i.e., circuit boards constructed with dovetail and oval male/female interlocking structures, the circuit boards having a semiconductor chip mounted thereon; col.2: 4-43) but does not teach a male interlocking element connector with two half parts, wherein one half part is inserted into a female interlocking element on one circuit board and the other half part is inserted into a female interlocking element on an adjacent circuit board.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
June 06, 2006